

## Dual-Band Wireless DPDT RF Switch

## DESCRIPTION

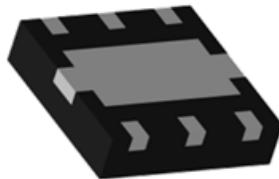
- The CG2164X3 is a GaAs MMIC DPDT (Double Pole Double Throw) switch for 2.5 GHz and 6 GHz dual-band wireless LAN applications

## FEATURES

- Control Voltage:  
VC(H) = 1.8 to 5.0 V (3.0V TYP.)  
VC(L) = -0.2 to 0.2 V (0V TYP.)
- Low Insertion Loss:  
 $L_{ins}$  = 0.50 dB TYP. @ f = 2.5 GHz  
 $L_{ins}$  = 0.60 dB TYP. @ f = 6.0 GHz
- High Isolation:  
ISL = 23 dB TYP. @ f = 2.5 GHz  
ISL = 15 dB TYP. @ f = 6.0 GHz
- Power Handling:  
 $P_{in}(0.5dB)$  = +32 dBm TYP. @ f = 2.5 GHz,  
VC(H) = 3.0 V, VC(L) = 0 V  
 $P_{in}(0.5dB)$  = +30 dBm TYP. @ f = 6.0 GHz,  
VC(H) = 3.0 V, VC(L) = 0 V

## PACKAGE

- 6-pin TSON Package  
(1.5mm x 1.5mm x 0.37mm)



## APPLICATIONS

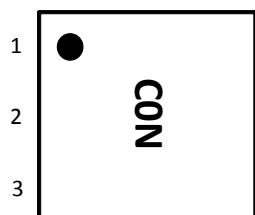
- Dual-band wireless LAN  
(IEEE802.11a/b/g/n/ac)

## ORDERING INFORMATION

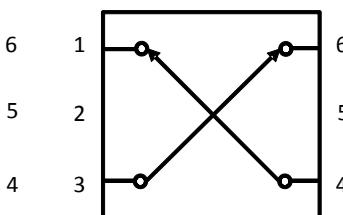
Part Number	Order Number	Package	Marking	Description
CG2164X3	CG2164X3-C2	6-pin plastic TSON (Pb-Free)	C0N	<ul style="list-style-type: none"><li>Embossed tape 8 mm wide</li><li>Pin 1, 6 face the perforation side of the tape</li><li>MOQ 10 kpcs/reel</li></ul>
CG2164X3-EVAL	CG2164X3-EVAL			<ul style="list-style-type: none"><li>Evaluation Board with DC block capacitors, power supply bypass capacitors, and RF and DC connectors</li><li>MOQ 1</li></ul>

## PIN CONFIGURATION AND INTERNAL BLOCK DIAGRAM

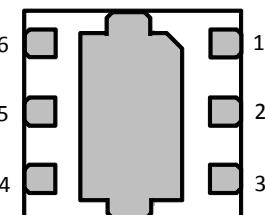
(Top View)



(Top View)



(Bottom View)



Pin No.	Pin Name
1	ANT2
2	VC2
3	RX
4	TX
5	VC1
6	ANT1

Remark Exposed pad : GND

## TRUTH TABLE

VC1	VC2	ANT1-TX	ANT1-RX	ANT2-TX	ANT2-RX
High	Low	OFF	ON	ON	OFF
Low	High	ON	OFF	OFF	ON

## ABSOLUTE MAXIMUM RATINGS

( $T_A = +25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Rating	Unit
Control Voltage	VC	6.0 <sup>Note 1</sup>	V
Input Power	$P_{in1}$	+33 <sup>Note 2</sup>	dBm
	$P_{in2}$	+26 <sup>Note 3</sup>	dBm
Operating Ambient Temperature	$T_A$	-45~+85	°C
Storage Temperature	$T_{stg}$	-55~+150	°C

**Note**

1.  $|\text{VC1} - \text{VC2}| \leq 6.0\text{V}$
2.  $3.0\text{V} \leq |\text{VC1} - \text{VC2}| \leq 5.0\text{V}$   $f \geq 0.5\text{GHz}$
3.  $3.0\text{V} \leq |\text{VC1} - \text{VC2}| \leq 5.0\text{V}$   $f \geq 0.05\text{GHz}$

## RECOMMENDED OPERATING RANGE

( $T_A = +25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Operating Frequency	$f$	0.05	-	6.0	GHz
Switch Control Voltage (H)	$\text{VC(H)}$	+1.8	+3.0	+5.0	V
Switch Control Voltage (L)	$\text{VC(L)}$	-0.2	0	+0.2	V

## ELECTRICAL CHARACTERISTICS 1

(TA=+25°C, VC(H)=3.0V, VC(L)=0V, Zo=50Ω, DC Block Capacitance=8pF, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Insertion Loss	Lins1	f = 0.05 to 0.5 GHz <sup>Note1</sup>	-	0.40	0.65	dB
	Lins2	f = 0.5 to 1.0 GHz <sup>Note1</sup>	-	0.45	0.70	dB
	Lins3	f = 1.0 to 2.0 GHz <sup>Note1</sup>	-	0.50	0.75	dB
	Lins4	f = 2.0 to 2.5 GHz	-	0.50	0.75	dB
	Lins5	f = 2.5 to 4.9 GHz	-	0.55	0.90	dB
	Lins6	f = 4.9 to 6.0 GHz	-	0.60	1.00	dB
Isolation (ANT to TX, RX)	ISL1	f = 0.05 to 0.5 GHz <sup>Note1</sup>	32	35	-	dB
	ISL2	f = 0.5 to 1.0 GHz <sup>Note1</sup>	26	29	-	dB
	ISL3	f = 1.0 to 2.0 GHz <sup>Note1</sup>	21	24	-	dB
	ISL4	f = 2.0 to 2.5 GHz	20	23	-	dB
	ISL5	f = 2.5 to 4.9 GHz	13	16	-	dB
	ISL6	f = 4.9 to 6.0 GHz	12	15	-	dB
Isolation (ANT1 to ANT2, TX to RX)	ISL7	f = 0.05 to 0.5 GHz <sup>Note1</sup>	34	37	-	dB
	ISL8	f = 0.5 to 1.0 GHz <sup>Note1</sup>	27	30	-	dB
	ISL9	f = 1.0 to 2.0 GHz <sup>Note1</sup>	22	25	-	dB
	ISL10	f = 2.0 to 2.5 GHz	22	25	-	dB
	ISL11	f = 2.5 to 4.9 GHz	15	18	-	dB
	ISL12	f = 4.9 to 6.0 GHz	15	18	-	dB
Return Loss	RL1	f = 0.05 to 2.0 GHz <sup>Note1</sup>	-	20	-	dB
	RL2	f = 2.0 to 6.0 GHz	-	15	-	dB
0.5 dB Loss Compression Input Power <sup>Note2</sup>	P <sub>in(0.5dB)</sub>	f = 0.05 GHz	-	+24.5	-	dBm
		f = 0.5 to 1.0 GHz	-	+31	-	dBm
		f = 2.4 to 2.5 GHz	-	+32	-	dBm
		f = 4.9 to 6.0 GHz	-	+30	-	dBm

**Note1** DC block capacitance = 1,000pF at f=0.05 to 2.0GHz

**Note2** P<sub>in(0.5dB)</sub> is the measured input power level when the insertion loss increases 0.5dB more than that of the linear range.

## ELECTRICAL CHARACTERISTICS 2

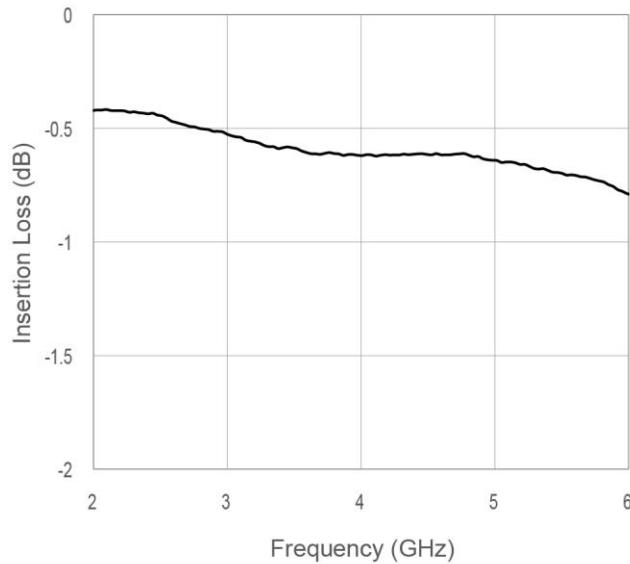
(TA=+25°C, VC(H)=3.0V, VC(L)=0V, Zo=50Ω, DC Block Capacitance=8pF, unless otherwise specified)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
2nd Harmonics	2f0	f = 2.5 GHz, Pin=+20dBm	-	85	-	dBc
		f = 6.0 GHz, Pin=+20dBm	-	80	-	dBc
3rd Harmonics	3f0	f = 2.5 GHz, Pin=+20dBm	-	85	-	dBc
		f = 6.0 GHz, Pin=+20dBm	-	85	-	dBc
3rd Order Input Intercept Point	IIP3	f = 2.5GHz 2-tone 1MHz Spacing	-	+55	-	dBm
Error Vector Magnitude	EVM	802.11a, 64QAM, 54Mbps, Pin≤+24.5dBm	-	2.5	-	%
		802.11g, 64QAM, 54Mbps, Pin≤+25dBm	-	2.5	-	%
Switch Control Speed	tsw	50% CTL to 90/10%	-	30	-	ns
Switch Control Current	Icont	Non RF	-	2	-	µA

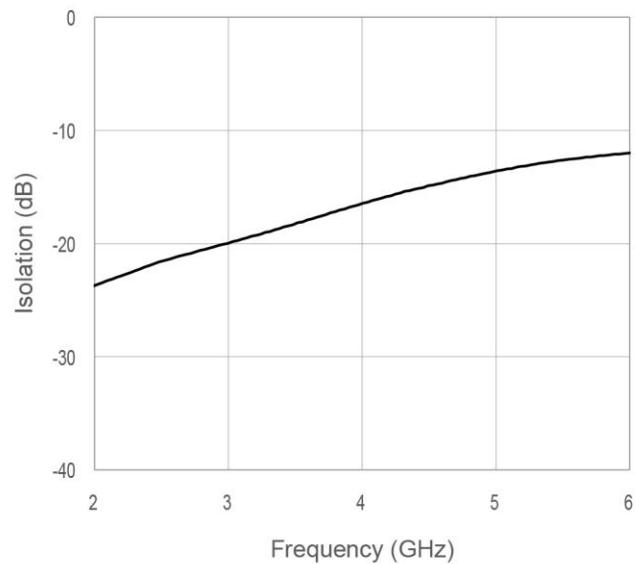
## TYPICAL CHARACTERISTICS

( $VC(H)=3V$ ,  $VC(L)=0V$ ,  $T_A = +25^{\circ}C$ , DC Block Capacitance=8pF, through board loss is subtracted in insertion loss data)

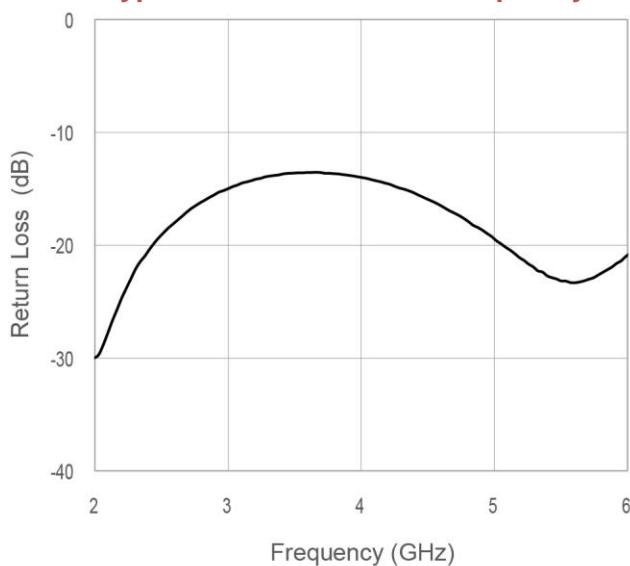
Typical Insertion Loss vs. Frequency



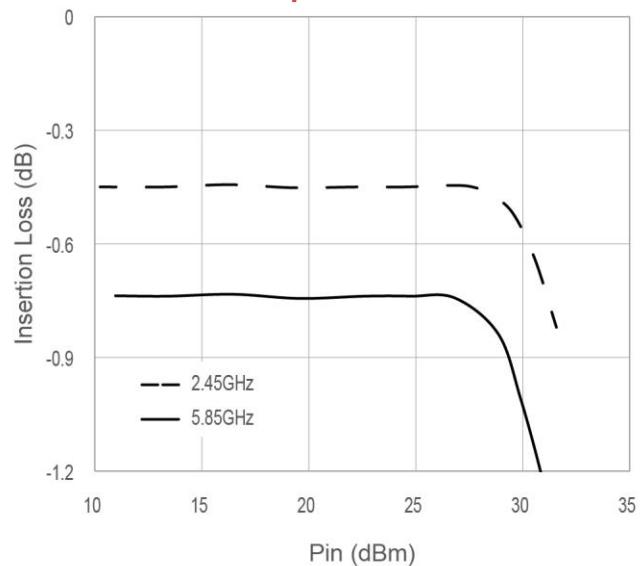
Typical Isolation vs. Frequency



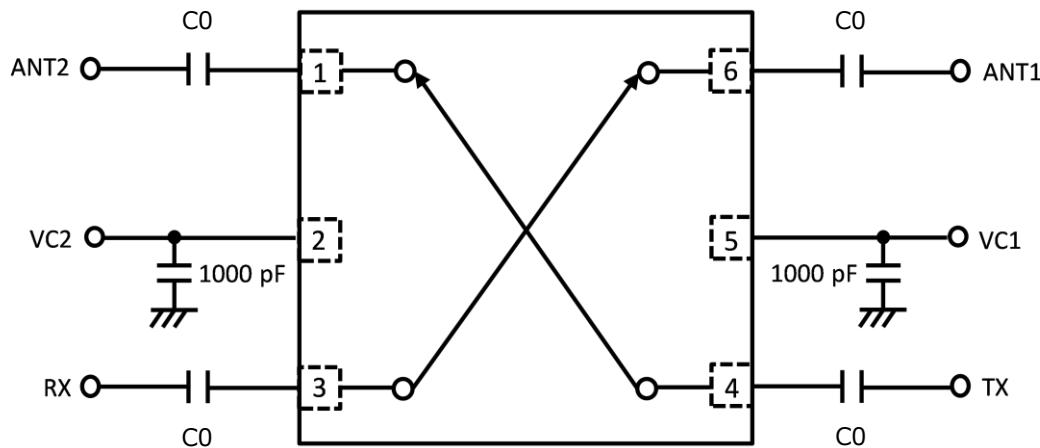
Typical Return Loss vs. Frequency



Typical Insertion Loss vs. Input Power



## EVALUATION CIRCUIT

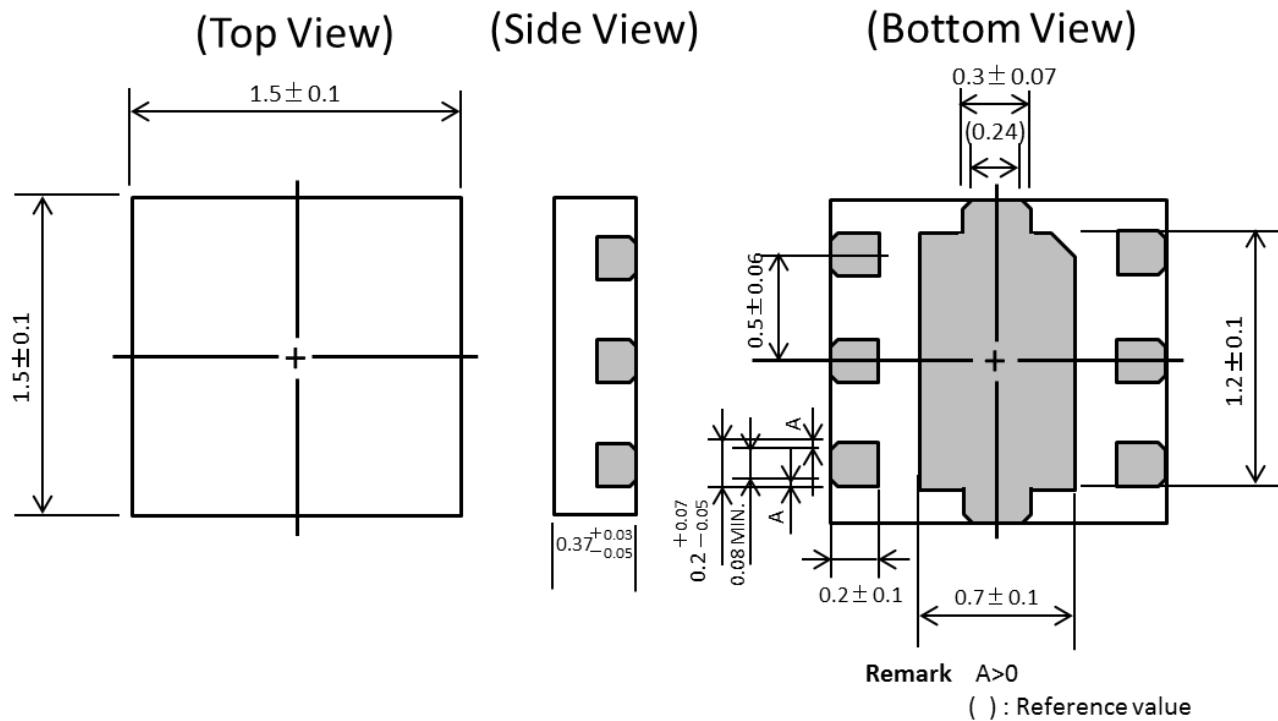


**Note** C0 : 0.05 to 2.0 GHz 1,000pF  
2.0 to 6.0 GHz 8pF

The application circuits and their parameters are for reference only and are not intended for use in actual designs.  
DC Blocking Capacitors are required at all RF ports.

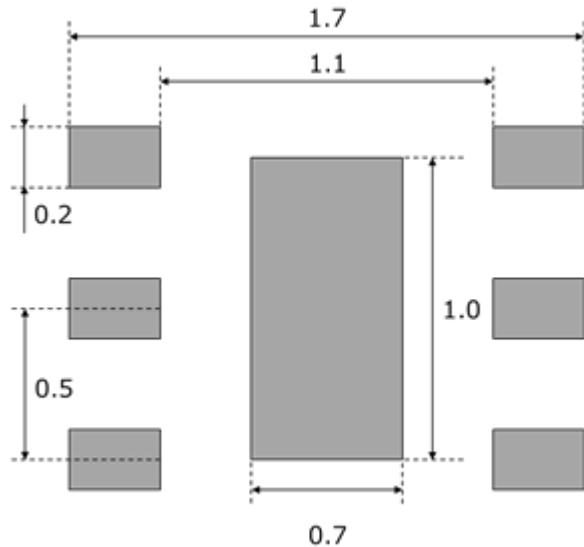
## PACKAGE DIMENSIONS

6-pin Plastic TSON (Unit: mm)



## PCB Layout Footprint

6-pin TSON (Unit: mm)



The PCB Layout Footprint In this document Is for reference only.

## RECOMMENDED SOLDERING CONDITIONS

Recommended Soldering Conditions are available on CEL's [Part Summary page](#) under Associated Documents

## REVISION HISTORY

Version	Change to current version	Page(s)
CDS-0033-01 (Issue A) September 14, 2016	Preliminary datasheet	N/A
CDS-0033-02 (Issue B) December 27, 2016	Revised Electrical Characteristics table Added “Recommended Soldering Conditions” section	3, 5
CDS-0033-03 (Issue C) March 20, 2017	Initial Datasheet. Revised Electrical Characteristics table	3
CDS-0033-05 (Issue D) August 28, 2017	Updated Characteristics tables and added Error Vector Magnitude Added “Typical Characteristics” graphs section Updated Evaluation Circuit diagram	3, 4, 5, 6
CDS-0033-06 (Issue E) October 25, 2017	Added PCB Layout Footprint	7

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